

Ishwar Suriyaprakash

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EDUCATION

University of California, Berkeley, B.A. Computer Science + Applied Mathematics (ML focus) 2024-2028

GPA: 4.0 / 4.0 *Dean's List – Fall '25, Spring '25*

Fall 2026 Courses: Computer Architecture / Machine Structures (RISC V), Machine Learning, Signals & Systems

Planned (Spring 2027): Digital Design & Integrated Circuits, Operating Systems

Prior Courses: Optimization Models in Engineering, Probability for Data Science, Data Structures, Structure & Interpretation of Computer Programs, Abstract Linear Algebra, Linear Algebra & Differential Equations, Honors Abstract Algebra, Real Analysis, Directed Reading – Representation Theory

WORK EXPERIENCE

Hardware Intern, System Technology, Apple

Jan 2026 – Aug 2026

- Developed machine learning methods for constrained placement of decoupling capacitors across Mac power rails, and evaluated with 4 metrics for placement legality, ground-truth proximity, and area utilization.
- Designed two placement approaches: (1) attention-GNN diffusion for simultaneous placement and (2) a 3-CNN ensemble for sequential placement.
- Developed software pipeline, Cadence Allegro → dataset extraction → model training → placement generation → evaluation, supporting both machine learning approaches.

Physical Design Intern, Machine Learning for Physical Design, Tenstorrent

May 2025 – Aug 2025

- Developed & integrated a dynamic IR-drop solver in an ML pipeline for power delivery network (PDN) generation for IR-drop-aware routing congestion reduction. Optimized dynamic IR-drop solver by leveraging current-waveform periodicity, peak structure, & parallelization, making closed-loop PDN optimization feasible.
- Evaluated ML-generated and human-designed PDNs using Ansys RedHawk-SC for IR drop; Enhanced place-and-route flow using Tcl to enable legal insertion of custom PDNs.

RESEARCH EXPERIENCE

Research Intern, Arizona State University

Advisor: Prof. Vidya Chhabria

2022-2024

- Developed voltage-aware static timing analyzer to model IR-drop-induced delay variation in digital circuits.
- Developed iterative and ML-based methods for PDN congestion reduction under IR-drop & timing constraints.
- Automated generation of synthetic Verilog netlists for model training and design-space experimentation.

Research Intern, UC Berkeley

Advisor: Prof. Alexander Strang.

Jan 2026 - present

- Developed rule-agnostic MLP models and training/evaluation pipeline to learn symmetric-game payoff structure from gameplay data within a visually interpretable framework.

SKILLS

Hardware: Static Timing & PDN/IR-drop Analysis, Innovus/Allegro, RedHawk-SC, OpenROAD, Verilog, NGSPICE

Machine Learning / Numerical Computing: PyTorch, PyTorch Geometric, TensorFlow, SciPy, scikit-learn, scikit-umfpack; Graph Neural Networks, Transformers, CNNs, U-Net, RNNs, MLPs, Diffusion Models, GANs

Languages / Scripting: Python, C++, Java, Linux Shell, Tcl, SQL, MATLAB, Scheme, Cadence SKILL

Agentic Development: Claude Code, Cursor; custom Claude Skills for workflow automation

Optimization: Linear Programming, Convex Optimization, Simulated Annealing, Metropolis-Hastings

SELECTED INDEPENDENT PROJECTS

- [Accelerated library cell characterization](#) for digital logic design using simulation-assisted machine learning
- Developed U-Net & Transformer models to identify landmark points on RC simulator aircraft images
- [Quantified finger fatigue](#) by frequency domain analysis of time series electromyography signals from muscles
- Developed semantic search for related-word & usage-trend queries using Google NGram, WordNet, hash maps, and directed graphs
- Grouping & generating music using autoencoders and generative adversarial networks

PUBLICATION & HONORS

- I. Suriyaprakash and G. Burroughs, "[DeepSPICE: Accelerating Digital Cell Characterization Using Deep Learning.](#)" *Journal of Student Research*, Vol. 11 No. 3 (2022).
- Intel Andy Grove Scholarship, 2026–27; Putnam top 13.2% (2025), top 20.5% (2024); USAPhO Bronze Medal (2023), Honorable Mention (2024); 4X AIME Qualifier (2020-24)